Claims 23-29 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the rejection, the Examiner stated:

> The method as recited is merely a flow chart of an idea to operate a processor. The steps as recited in the claim combination are not actually performed by the processors such that a meaningful result is achieved. The method steps actually are reciting the architectural structure (see the first four steps of claim 23) of a processor and the functions (see the last two steps of claim 23) of the components thereof.

In response, Applicants respectfully contend that the above rejection is improper under MPEP2173.05(v). MPEP2173.05(v) [Mere Function of Machine] states:

> In view of the decision of the Court of Customs and Patent Appeals in *In re Tarczy-Hornoch*, 39 F.2d 856, 158 USPQ 141 (CCPA 1968), process or method claims are not subject to rejection by Patent and Trademark Office examiners under 35 USC 112, second paragraph, solely on the ground that they define the inherent function of a disclosed machine or apparatus. The court in re Tarczy-Hornoch held that a process claim, otherwise patentable, should not be rejected merely because the application of which it is part discloses apparatus which will inherently carry out the recited steps.

Claims 23-29 state:

> 23. A method of operating a processor comprising:
> operating a plurality of functional units; and
> dividing a register file into a plurality of register file segments;
> coupling and associating ones of the plurality of register file segments with ones of the plurality of functional units;
> partitioning the register file segments into global registers and local registers;
> accessing the global registers by the plurality of functional units;
> accessing the local registers by the functional unit associated with the register file segment containing the local registers.
> 24. A method according to Claim 23 further comprising:

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addressing the local registers and global registers using register addresses in an address space that is defined for a register file segment/ functional unit pair.

25. A method according to Claim 23 further comprising:
addressing the local registers in a register file segment using register addresses in a local register range outside the global register range that are assigned within a single register file segment/ functional unit pair.

26. A method according to Claim 23 further comprising:
addressing the local register range the same for the plurality of register file segment/ functional unit pairs and address registers locally within a register file segment/ functional unit pair.

27. A method according to Claim 23 further comprising:
including N physical registers in the register file;
duplicated the physical registers into M register file segments, the register file segments having a reduced number of read and/or write ports in comparison to a nonduplicated register file, but each having the same number of physical registers.

28. A method according to Claim 27 further comprising:
partitioning the register file segments into NG global and NL local register files where NG plus NL is equal to N;
operating the register file equivalently to a register file having NG + (M * NL) total registers available for the M functional units, the number of address bits for addressing the NG + (M * NL) total registers being equal to the number of bits B that are used to address N = 2B registers; and
addressing the local registers for ones of the M register file segments using the same B-bit values.

29. A method according to Claim 27 further comprising:
programmably partitioning the register file so that the number NG of global registers and number NL of local registers is selectable and variable.

The above claims clearly fall within the rubric of MPEP2173.05(v) in that method claims are not subject to rejection solely on the ground that they define the inherent function of the disclosed apparatus. Therefore, for the above reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections of Claims 23-29 under 35 U.S.C. § 112, second paragraph.

Claims 1-29 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yung

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(U.S. 5,592,679) in view of Nishimoto (U.S. 6,023,757). In the rejection, the Examiner stated:

> Yung discloses a system having a plurality of processors and a global register which is shared by the processors. Each of the processors further includes its own local register which can be accessed by the associated processor only. Yung does not show that each of the processor also includes a decoder for decoding VLIW. Decoder and VLIW are well-known in the art. Nishimoto shows in Figure 1 a processing system having a local register (line 64, col. 5), in Figure 2 a processing system having a global register (line 35, col. 7). Both systems also include a decoder for decoding VLIW (see abstract). From the teaching of Nishimoto, it would have been obvious to a person of ordinary skill in the art to incorporate a decoder in Yung such that VLIW can be executed.

In response, Applicants respectfully contend that not only do the combined references fail to show the features of the claimed invention but the obviousness rejection under 35 U.S.C. § 103 cannot be established by combining the teachings of Yung and Nishimoto because there is no suggestion or motivation in the cited references for combining Yung and Nishimoto. "For a proper obviousness combination, the prior art references must provide a suggestion or motivation to make such a combination." Heidelberger Druckmaschinen AG v. Hantscho Commercial Prods., Incs., 21 F.3d 168, 1072, 30 USPQ2d 1377, 1379 (Fed. Cir. 1994) *citing* Northern Telecom Inc. v. Datapoint Corp., 908 F.2d 931, 934 15 USPQ2d 1321, 1323 (Fed. Cir. 1990).

Yung discloses a single DDF processor 200, and a global register file 290. There is no mention that a plurality of processor share a single global register file. The processor includes local register buffers (241d, 242d). Yung discloses a multi-level instruction scheduling system for controlling multiple execution pipes of a distributed data flow processor. (Yung,

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Abstract, col. 2, lines 65-67). However, there is no mention that a register file is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers., as is being claimed by Applicant. Furthermore, Yung teaches a different method from Applicant in that Yung teaches a multi-level instruction scheduling system for controlling multiple execution pipes of a distributed data flow processor. (Yung, Abstract, col. 2, lines 65-67). Yung teaches away from the claimed invention in that Yung states that "[a] single centralized register file is not ideal because interconnecting the large fast global memory to a large number of execution units is prohibitively expansive in silicon area and requires extremely complex circuitry with many I/O ports." The claimed invention includes a single centralized register file. Yung is classified in class 712, subclass 23. Therefore, Yung is directed to solving the problem of a superscalar processor in that it is "subject matter comprising an architecture which determines a group of upcoming instructions which do not mutually interfere with each other and issue or dispatches this group simultaneously" (See Class Definitions, Class 712, Subclass 23). Thus, Yung teaches a multi-level instruction scheduling system for controlling multiple execution pipes of a distributed data flow processor (Yung, Abstract, col. 2, lines 65-67) while Applicant teaches storage having local and global access regions for subinstructions in a Very Long Instruction Word (VLIW) processor (Specification, page 1, lines 7-8).

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As admitted by the Examiner, Yung does not teach the use of a decoder for decoding VLIW nor does it teach a processor having a plurality of functional units including a multi-ported register file that is divided into a plurality of separate register file segments, each of the register file segments being associated to one of the plurality of functional units where the register file segments are partitioned into local registers and global registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers.

On the other hand, while the invention disclosed in Nishimoto relates generally to a microprocessor or microcomputer (col. 1, lines 4-5) and specifically to a method and apparatus for use in a data processor to cause the data processor to attain high-speed performance while maintaining software compatibility (col. 1, lines 5-9), Nishimoto is directed to addressing a completely different problem than Yung. Yung was addressed to solving the problem of a multi-level instruction scheduling system for controlling multiple execution pipes of a distributed data flow processor. (Yung, Abstract, col. 2, lines 65-67). Nishimoto, on the other hand, discloses a method for causing a data processor to attain high-speed performance while maintaining software compatability (col. 1, lines 5-9). There is no suggestion in Yung that a processor include a plurality of functional units; and a register file that is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers, the global registers that are accessible by the plurality of functional units, the local registers being

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accessible by the functional unit associated with the register file segment containing the local registers, is desirable nor does Nishimoto suggest a combination of its joint processing technique with the instruction grouping and dispatching technique of Yung. Nishimoto is classified in class 712, subclass 209. Therefore, Yung is directed to solving the problem of decoding instructions to accommodate plural instruction interpretations (See Class Definitions, Class 712, Subclass 209) while Applicant teaches storage having local and global access regions for subinstructions in a Very Long Instruction Word (VLIW) processor (Specification, page 1, lines 7-8). The claimed invention teaches a processor including a plurality of functional units; and a register file that is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers. Neither Yung, Nishimoto or the references combined teach the claimed invention.

Obviousness is tested by "what the combined teachings of the references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). But obviousness "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." ACS Hosp. Sys. Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). Thus, "teachings of references can be combined only if there is some suggestion or incentive to do so." Id. Applicants, thereby, contend that

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there is no suggestion or incentive to combine Yung and Nishimoto because Yung and Nishimoto are directed to solving different problems with different solutions, as outlined above.

Thus, for a obviousness combination, the "critical inquiry is whether 'there is something in the prior art as a whole to suggest the desirability, and thus the obviousness of making the combination.'" Fromson v. Advance Offset Place, Inc., 755 F.2d 1549, 1556, 225 USPQ 26, 31 (Fed. Cir. 1985) *quoting* Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1453, 1452, 221 USPQ 481, 488 (Fed. Cir. 1984). In other words, the "mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." In re Gordon, 773 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) *citing* Carl Schenck, A.G. v. Nortron Corp., 713 F.2d 782, 787, 218 USPQ 698, 702 (Fed. Cir. 1983). Yung does not suggest the desirability of a combination with Nishimoto because, as mentioned above, Yung and Nishimoto are directed toward different problems with different solutions. Accordingly, Yung does not suggest to one skilled in the art the desirability to search for other ways that improve storage such that the storage has local and global access regions for subinstructions in a Very Long Instruction Word (VLIW) processor, much less for a combination with a reference having a different problem and different solution, such as Nishimoto.

Furthermore, the "statute, §103, requires much more, i.e., that it would have been obvious to produce the claimed invention at the time it was made without the benefit of hindsight." Orthokinetics, Inc. v. Safety Travel, Chairs, Inc., 806 F.2d 1565, 1575, 1 USPQ2d 1081, 1087 (Fed. Cir. 1986). "When prior art references require selective

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combination by the court to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself." Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985) *citing* ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577 & n.14, 221 USPQ 929, 933 & n.14 (Fed. Cir. 1984). Applicants believe the motivation to combine Yung with Nishimoto is derived from Applicants' invention since there is no suggestion in the cited references for the desirability of such a combination. The instant application is directed to a processor including a plurality of functional units; and a register file that is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers.

Examiner's 103 rejection of Claims 1-29 was also procedurally inadequate as the rejection failed to provide any basis for combining Yung and Nishimoto and also failed to show that the combined prior art references teach or suggest *all claim limitations*. The Examiner merely stated that:

> Yung discloses a system having a plurality of processors and a global register which is shared by the processors. Each of the processors further includes its own local register which can be accessed by the associated processor only. Yung does not show that each of the processor also includes a decoder for decoding VLIW. Decoder and VLIW are well-known in the art. Nishimoto shows in Figure 1 a processing system having a local register (line 64, col. 5), in Figure 2 a processing system having a global register (line 35, col. 7). Both systems also include a decoder for decoding VLIW (see abstract). From the teaching

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> of Nishimoto, it would have been obvious to a person of ordinary skill in the art to incorporate a decoder in Yung such that VLIW can be executed.

With all due respect, the Examiner failed to provide any explanation as to what was the suggestion or motivation in the references rendering it obvious to use a processor that includes a decoder for decoding VLIW, allegedly to be found within Nishimoto, in the processor, global and local register file of Yung. Additionally, the Examiner's rejections appeared to only address independent claims 1, 15 & 23 and failed address the features of dependent claims 2-14, 16-22 & 24-29. MPEP 706.02(j) [Contents of a 35 USC 103 Rejection] clearly spells out the criteria an Examiner must meet in order to issue a rejection under 35 USC 103:

> 35 USC 103 authorizes a rejection where, to meet the claim, it is necessary to modify a single reference or to combine it with one or more other references. After indicating that the rejection is under 35 USC 103, the examiner should set forth in the Office action:
>
> (A) the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate,
>
> (B) the difference or differences in the claim over the applied reference(s),
>
> (C) the proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and
>
> (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification.
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, *there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.* Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined)

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must teach or suggest *all claim limitations*. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143-2143.03 for decisions pertinent to each of these criteria.

The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Capp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). See MPEP 2144-2144.09 for examples of reasoning supporting obviousness rejections.

Where a reference is relied on to support a rejection, whether or not in a minor capacity, that reference should be positively included in the statement of rejection. See *In re Hoch*, 428 F.2d 1341, 1342 n.3 166 USPQ 406, 407 n.3 (CCPA 1970).

It is important for an examiner to properly communicate the basis of a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply. Furthermore, if an initially rejected application issues as a patent, the rationale behind an earlier rejection may be important in interpreting the scope of the patent claims. Since issued patents are presumed valid (35 USC 282) and constitute a property right (35 USC 261), the written record must be clear as to the basis for the grant. Since patent examiners cannot normally be compelled to testify in legal proceedings regarding their mental processes (See MPEP 1701.01), it is important that the written record clearly explain the rationale for decisions made during prosecution of the application. [emphasis added]

Therefore, because Applicants contend that the combination of Yung and Nishimoto was both substantively and procedurally improper, Applicants respectfully request reconsideration and withdrawal of the rejections to Claims 1-22 under 35 U.S.C. § 103(a).

Claims 1-29 were provisionally rejected under the judicially created doctrine of double

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patenting over claim 1-22 of copending Application No. 09/204,479 in view of Yung (U.S. 5,592,679). In the rejection, the Examiner stated:

> The claims of copending applications recite a system having a plurality of functional units and a register file. The copending claims do not specify whether the registers are of global and local type. Yung teaches both types of registers. It would have been obvious to a person of ordinary skill in the art to incorporate a global register in the system of copending application such that the processors are able to share information via global registers.
>
> This is a provisional obviousness-type double patenting rejection.

In response, Applicants respectfully contend that the provisional rejection under the judicially created doctrine of double patenting over claim 1-22 of copending Application No. 09/204,479 in view of Yung (U.S. 5,592,679) is procedurally improper. As the rejections are procedurally improper, it is not necessary to address the substantive issues presented by the provisional rejections. Arguendo, and without waiver of the above, on a substantive level, Applicants recognize the provisional nature of the rejections, and will address the substantive aspect of this issue in future communications to this Office should Claims 1-22 of copending Application No. 09/204,479 be allowed at some future point in time and in the same, or substantially the same, form as they now presently exist. However, as a procedural matter, MPEP 706.02(k) [Provisional Rejection (Obviousness) Under 35 USC 102(e)/103] states that:

> Where two applications of different inventive entities are copending and the filing dates differ, a provisional rejection under 35 USC 102(e)/103 should be made in the later filed application if the applications have a common assignee or a common inventor. [emphasis added] See MPEP, 7th Edition, Rev. 1.

The instant application was filed on December 3, 1998 and assigned Application No.

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09/204,585. Copending application No. 09/204,479 was also filed on December 03, 1998. As both applications were filed on the same day, neither application was filed earlier or later than the other. Therefore, according to MPEP 706.02(k), it is respectfully presented that the instant rejection of claims 1-29 is procedurally improper *as the instant application is not the later filed application.* Therefore, for the above reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections of Claims 1-29 under the judicially created doctrine of obviousness-type double patenting based on claims 1-22 of copending Application No. 09/204,479 in view of Yung (U.S. 5,592,679).

CONCLUSION

For the foregoing reasons, Applicant believes the pending Claims 1-29 are allowable, and a Notice of Allowance is respectfully requested. The Examiner is invited to call the Applicants' Attorney at (949) 718-6780 for any questions with this response.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on October 19, 2000.

Attorney for Applicant(s) — Date of Signature: 10/19/00

Respectfully submitted,

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